TRSF16128A(B)

Data Sheet

V2.2

128K Embedded Flash

Hi-Performance 16-bit Speech Processor

1. General Description

The **TxP16S**™ is a high performance 16-bit MCU, running up to 32MHz and provided with 128K FLASH and total 4K SRAM for high performance process of audio algorithm. It is the new generation computational kernel for **TRITAN** Flash Speech series. It has initially aimed at the areas of speech application to demonstrate its profession. TxP16S furnish with a fast unit, which allows calculation instructions to be issued with access memory simultaneously during one cycle. The TRSF16128A is equipped with TxP16S and integrating input/output ports, Audio PWM/DAC, Timer and Low Voltage Reset...etc on a chip.

Furthermore, TRSF16128A extend its external device connection capability such as Serial ROM/Flash. The internal memory capacity includes 128Kx16 program/data FLASH plus 4Kx16 working SRAM.

2. Features

- ***TRSF16128B(only one package : SOP16-2)***
- High-performance RISC TxP16S CPU
  - wide working frequency and voltage 4Mhz ~32Mhz@2.2Volt ~ 5.5Volt
  - Operation frequency is programmable by Software
  - Built-in 4096x16 SRAM
  - Embedded PC Stack Level 16
- Embedded Flash 128Kx16
  - Typical 1,000 erase/program cycles
  - Greater than 10 years Data Retention
- Software-based audio processing technical
  - Subband , ADPCM , Melody
- Support 22+2(ICE PAD can be as I/O) general purpose I/O port.
- Mono 16bit PWM or 14bit DAC
- 6 IRQ include 2 external interrupt
- SPI Master interface
- Three timers: Timer1, Timer2, RTC timer
- Support Spread Spectrum clocking to reduce EMI.
- Watch dog timer (WDT)
- Low voltage reset (LVR)
- PB0, PB1, PB2, PB3 support two edge modes for wake-up function are rising and falling edge trigger.
- 2 channel comparators and a two stage OPA with class AB output
- Microphone with AGC(Auto Gain Control)
- IR
- Low voltage detector
- Buzzer and speaker wake up
- ***VCC Decoupling Cap 33uF should be close to IC within 0.5cm.***
- ***Power Path of VCC and VSS must pass through Decoupling Cap 33uF into IC.***
- ***Power Path of VPD and VCC must pass through Resistor 33Ω into IC.***

3. Application Field

- MCU Application
- Electronic Dictionary
- Handheld Games
- Electronic Learning Aid (ELA)
- Electronics storybook

4. Block Diagram

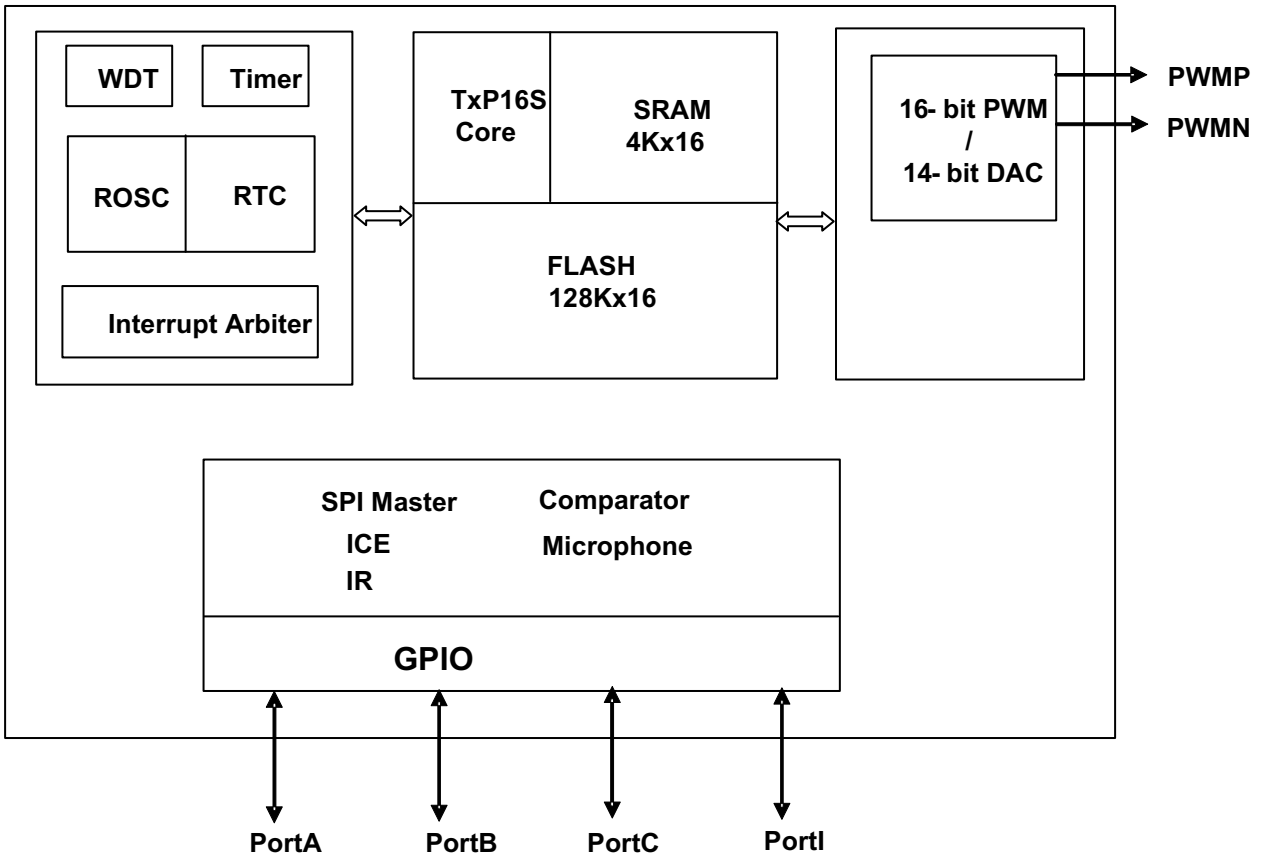

Figure 4.1

4.1 Pin Assignments /Description

Pin Name	I/O	State after RESET	FUNCTIONS
Chip Power			
VCC	I	High	Chip Power Input
VSS	I	Low	Digital Ground
VPD	I	High	PWM IO PAD Power Input
VPS	I	Low	PWM IO PAD Ground
General Purpose I/O Port			
PortA[3:0]	I/O	Low	PortA is programmable Input/Output port
PortB[5:0]	I/O	Low	PortB is programmable Input/Output port
PortC[11:0]	I/O	Low	PortC is programmable Input/Output port PortC[2] is programmable Input/Output port when not connected to ICE ICE_VPP: PortC[2] is embedded ICE VPP pin when connected to ICE Probe.
PortI[1]/ ICE_SCLK	I/O	Low	PortI[1] is programmable Input/Output port when not connected to ICE Probe. Internal pull-down R (50K ohm) will be enable at ICE mode. ICE_SCLK: PortI[1] is embedded ICE clock pin when connected to ICE Probe.
PortI[0]/ ICE_SD	I/O	Low	PortI[0] is programmable Input/Output port when not connected to ICE Probe. Internal pull-down R (50K ohm) will be enable at ICE mode. ICE_SD: PortI[0] is embedded ICE data pin when connected to ICE Probe.
PWM Audio			
PWMP	O	Low	Digital PWM output(+) / Analog DAC output(+)
PWMN	O	Low	Digital PWM output(-) / Analog DAC output(-)

16. SPI Operation Sequence:

A1.0 Initial Process

```
set io[IOC_PB].b5          // set output port
set io[STATUS].b8          // Enable SPI Control

set io[PortB].b5           // CS=1
ar = io[SPI_CTRL]
set   ar.b11               // set ICS = 1
io[SPI_CTRL] = ar
```

A1.1 Sending Data Process

```
clr io[PortB].b5             // CS =0
ar = io[SPI_CTRL]
clr   ar.b11                 // ICS = 0
io[SPI_CTRL] = ar
```

```
SPI_write_data:
        ar = data
         io[SPI_DATA] = ar;          // write data

         ar = 0x12;                  // set total byte number & send data
         ah = 0x10;                  // speed 16M
         io[SPI_CTRL] = ar;          //set SEND = 1;
         call   Check_Tran_OK

         set io[PortB].b5            // CS =1
         ar = io[SPI_CTRL]
         set   ar.b11                // ICS = 1
         io[SPI_CTRL] = ar
```

```
Check_Tran_OK:
          ar = io[SPI_CTRL]
          test   ar.b7
           if eq jmp Check_Tran_OK
Check_Tran_OK_End:
          rets
```

A1.2 Receiving Data Process

```
clr io[PortB].b5                // CS =0
ar = io[SPI_CTRL]
clr   ar.b11                    // ICS = 0
io[SPI_CTRL] = ar

SPI_read_data:
ar = 0x22;                      // set total byte number & receive data
ah = 0x10;                      // speed 16M
io[SPI_CTRL] = ar;              //set RCV = 1;
call   Check_Tran_OK
ar = io[SPI_DATA];              // read data

set io[PortB].b5                // CS =1
ar = io[SPI_CTRL]
set   ar.b11                    // ICS = 1
io[SPI_CTRL] = ar


Check_Tran_OK:
ar = io[SPI_CTRL]
test   ar.b7
 if eq jmp Check_Tran_OK
Check_Tran_OK_End:
rets
```

17. Revision history

REVISION	DESCRIPTION	PAGE	DATE
V1.0	New establish		2018/6/20
V1.1	Add 9-2 ~ 9-5 sector	28~33	2018/6/28
V1.2	Add Power Line PCB Layout Guide	40~41	2018/9/26
V1.3	Modify Fbank2 to Fbank7	36	2018/10/30
	Modify Microphone Circuit	31~32	
	Add DAC mode	25	
	Change working voltage 2.2Volt ~ 5.5Volt	36	
	At DAC mode, the working frequency range of BANK0 (Flash memory) is from 4MHz to 8MHz.	3, 36	
	At PWM mode, the working frequency range of BANK0 (Flash memory) is only up to 4MHz.	3, 36	
	At DAC mode, resistor 33Ω can be removed and VPD is directly shorted to VCC.	3, 37, 40	
	At PWM mode, resistor 33Ω must be needed and VPD connects the resistor 33Ω to VCC.	3, 37, 40	
V2.0	Modify SOP16 Package	42	2018/12/18
	Modify Microphone Circuit	31~32	
	Add SPI Operation Sequence	43~44	
	Modify Notice	3, 36, 37, 40, 41	
	Remove SPI Clock 32.768M	22	
	Add Dynamic System Clock	28	
V2.1	Add SSOP24 Package	44	2019/5/2
	Modify GPIO VIH/VIL	38	
	Add Touch Controller	25, 26	
V2.2	Add TRSF16128B(only one package : SOP16-2)	44	2019/7/25
	Remove RXEN	8, 10	